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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,160	FRIESE, GERALD	
	Examiner	Art Unit	
	Matthew J. Song	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/17/2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al (US 6,159,826).

Kim et al discloses a conductive, metal line **52a** of an internal circuit (col 2, ln 5-10 and col 3, ln 35-36), this reads on applicant's metal layer. Kim et al also discloses a conductive region **55** fills a via hole formed in a first insulating layer **53**, where the first insulating layer reads on applicant's dielectric and the conductive region reads on applicant's interconnect. Kim et al also discloses a bond pad **56** having a first portion **56a** disposed over the metal layer and the

interconnect, and a second portion **56b** disposed over the dielectric layer (col 3, ln 45-55 and Fig 5). Kim et al also discloses a first portion including a bond pad **36** for providing an attachment point for a connection (col 1, ln 20-35) and a second portion including a probing pad **38** for contact with a probe **60** (col 3, ln 45-67). Kim et al also discloses a second insulating layer **57**, this reads on applicant's passivation layer, from on the first insulating layer **53** and the first portion **56a** and the second portion **56b** are exposed out the second insulating layer, this reads on applicant's passivation layer includes a first opening and a second opening.

Referring to claim 1, Kim et al discloses a probe pad area **56b**, which is separated from the bond pad area **56a** by an insulating layer **57** (Fig 5), this reads on applicant's bond area is separated from the probe area. Kim et al also discloses the probe pad area **56b** does not overlie the metal line **52a** and overlies an insulating layer **53** (Fig 5), this reads on applicant's second portion is disposed over the dielectric layer and offset from the metal line. Furthermore, the portion of layer **56a**, which does not overlie the metal line **52a** (Figs 5-6 and 9) reads on applicant's probe pad disposed over a dielectric and offset from a metal line because a bond pad can also function as a probe pad, as evidenced by page 3 of the instant specification.

Referring to claim 8, Kim et al discloses a separate probe area and bond area. However, the bond area can inherently be used as a probe area, note page 3 of the instant specification; therefore the bond area opening inherently includes a probe area.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 10, 12, 15, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136).

Kim et al discloses all of the limitations of claim 4, as discussed previously, except a barrier layer disposed between the interconnect and the metal layer to prevent diffusion therebetween.

In a method of making a semiconductor device with a bond pad region, note entire reference, Yoshioka teaches a metal layer **15** formed of a refractory metal (col 4, ln 45-50), an interconnect **19** formed through a oxide insulator, which may contain phosphorus or boron **14** connecting to the metal layer (col 4, ln 55-60), and a bond pad **30** (col 4, ln 15-25 and col 5, ln 20-25). Yoshioka also teaches the barrier metal layer may consist of TiN, TiW, or W (col 4, ln 1-10). Yoshioka also teaches a barrier metal layer serves to prevent solid phase epitaxy in the opening of an integrated circuit device employing a conductive pattern (col 1, ln 30-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by employing the barrier metal layer taught by Yoshioka to prevent solid phase epitaxy ('136 col 1, ln 30-40).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Cheung et al (US 5,785,236) or Zawaideh (US 5,877,557).

Kim et al teaches all of the limitations of claim 1, as discussed previously, except the bond pad include aluminum.

In a method of wire bonding for integrated circuits, note entire reference, Cheung et al teaches a metal interconnect formed over an integrated circuit structure, forming an aluminum pad over the metal interconnect and bonding a metal wire to the aluminum pad (col 2,ln 50 to col 3, ln 5). Cheung et al also teaches a layer of conventional aluminum is patterned to form at least one aluminum pad (col 3, ln 40-55). Cheung et al also teaches an insulating layer or passivating layer is formed on the aluminum pad and patterned to expose the surface of the pad (col 3, ln 56-67). Cheung et al also teaches wire bonding to the pad (col 4, ln 10-25). Cheung et al also teaches bonding pad openings are formed in a passivation layer (col 3, ln 60-67). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using the aluminum pad taught by Cheung et al because the selection of a known material based on its suitability for its intended use is held to be obvious (MPEP 2144.07).

In a method of making a semiconductor device, note entire reference, Zawaideh teaches aluminum is often used as a conductive metal in semiconductor devices (col 1, ln 10-15) and aluminum is used in integrated circuits to form aluminum plugs, aluminum interconnects, aluminum bonding pads and other such structures (col 2, ln 15-20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using the aluminum pad taught by Zawaideh because the selection of a known material based on its suitability for its intended use is held to be obvious (MPEP 2144.07).

7. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Wood et al (US 6,107,122).

Kim et al teaches all of the limitations of claim 5, as discussed previously, except the bond pad has a thickness of less than 2 microns.

In a method of making a semiconductor device, note entire reference, Wood et al teaches typical aluminum bond pads having a thickness of from 1.0 to 1.5 μm (col 5, ln 25-26). Wood et al also teaches electrodes can comprise thin film aluminum bond pads in electrical communication with integrated circuits (col 5, ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using the aluminum pad with a thickness of 1.0 to 1.5 μm taught by Wood et al because the thickness is conventionally used in the art for bonding pads.

Referring to claim 5, the combination of Kim et al and Wood et al teaches a bond pad thickness of 1.0-1.5 μm. Overlapping ranges are held to be obvious (MPEP 2144.05).

8. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Admission (Applicant's admitted prior art).

Kim et al teaches all of the limitations of claim 2, as discussed previously, except the metal layer includes copper.

In applicant's admitted prior art, Admission teaches copper metallizations are employed due to their high conductivities and aluminum is used as cap. Admission also teaches copper metallization for metal lines and an aluminum bond pad. Admission also teaches a diffusion

barrier, which may include Ta or TaN is deposited between the copper and aluminum to prevent diffusion therebetween (page 1-3 of the instant specification).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using a copper metal layer and an aluminum bond pad because the selection of a known material based on its suitability for its intended used is held to be obvious (MPEP 2144.07).

Referring to claim 4, Kim et al does not teach a diffusion barrier. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al with Admission diffusion barrier to prevent diffusion between copper and aluminum, which is detrimental to resistivity (page 2 of Admission).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Cain (US 5,656,945).

Kim et al teaches all of the limitations of claim 9, as discussed previously, except the bond pad is permanently connected to a bond wire.

In a method of testing electrical device, Cain teaches mounting a die within a package typically involves attaching a die with a socket formed in the package and permanently attaching package leads to the wire bond pads, by wire bonding, lead bonding or soldering, this reads on applicant's bond pad is permanently connected to a bond wire (col 2, ln 1-25). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by permanently connecting a package lead to a bond pad to form a package, which can be tested (col 1, ln 45-67).

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136) as applied to claim 10 above, and further in view of Wood et al (US 6,107,122).

The combination of Kim et al and Yoshioka teaches all of the limitations of claim 14, as discussed previously, except the bond pad with a thickness of less than about 2 microns.

In a method of making a semiconductor device, note entire reference, Wood et al teaches typical aluminum bond pads having a thickness of from 1.0 to 1.5 μm (col 5, ln 25-26). Wood et al also teaches electrodes can comprise thin film aluminum bond pads in electrical communication with integrated circuits (col 5, ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kim et al and Yoshioka by using the aluminum pad with a thickness of 1.0 to 1.5 μm taught by Wood et al because the thickness is conventionally used in the art for bonding pads.

Referring to claim 5, the combination of Kim et al, Yoshioka and Wood et al teaches a bond pad thickness of 1.0-1.5 μm. Overlapping ranges are held to be obvious (MPEP 2144.05).

11. Claims 11-13, 18-19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136) as applied to claim 10 above, and further in view of Admission (Applicant's admitted prior art).

The combination of Kim et al and Yoshioka teaches all of the limitations of claim 11, as discussed previously, except the metal layer includes copper.

In applicant's admitted prior art, Admission teaches copper metallizations are employed due to their high conductivities and aluminum is used as cap. Admission also teaches copper metallization for metal lines and an aluminum bond pad. Admission also teaches a diffusion barrier, which may include Ta or TaN is deposited between the copper and aluminum to prevent diffusion therebetween (page 1-3 of the instant specification).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al or Yoshioka by using a copper metal layer and an aluminum bond pad because the selection of a known material based on its suitability for its intended used is held to be obvious (MPEP 2144.07).

Referring to claims 13 and 19, the combination of Kim et al and Yoshioka teaches using a barrier layer. The combination of Kim et al and Yoshioka does not teach a diffusion barrier includes Ta or Tan. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al with Admission diffusion barrier of Ta or TaN to prevent diffusion between copper and aluminum, which is detrimental to resistivity (page 2 of Admission).

Referring to claim 18, the combination of Kim et al, Yoshioka and Admission teaches a copper metal line (Admission pg 3 and '826 col 2, ln 5-10), an insulating layer **53** formed over the circuit **52**, this reads on applicant's dielectric, a diffusion barrier (Admission page 2 and '136 col 3, ln 65 to col 4, ln 15), an aluminum interconnection which defines a binding pad over openings and the conductive layer ('4, ln 15-25), first area and a second area ('136 Fig 1 and '826 Fig 5).

Referring to claim 21, the combination of Kim et al, Yoshioka and Admission teaches a second insulation layer **57** ('826 col 3, ln 45-55) and a protection layer **20** ('136 col 5, ln 10-25), which reads on applicant's passivation layer.

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136) and Admission (Applicant's admitted prior art), as applied to claim 18 above, and further in view of Wood et al (US 6,107,122).

The combination of Kim et al, Yoshioka and Admission teaches all of the limitations of claim 20, as discussed previously, except the bond pad with a thickness of less than about 2 microns.

In a method of making a semiconductor device, note entire reference, Wood et al teaches typical aluminum bond pads having a thickness of from 1.0 to 1.5 μm (col 5, ln 25-26). Wood et al also teaches electrodes can comprise thin film aluminum bond pads in electrical communication with integrated circuits (col 5, ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kim et al, Yoshioka and Admission by using the aluminum pad with a thickness of 1.0 to 1.5 μm taught by Wood et al because the thickness is conventionally used in the art.

Referring to claim 5, the combination of Kim et al, Yoshioka, Admission and Wood et al teaches a bond pad thickness of 1.0-1.5 μm. Overlapping ranges are held to be obvious (MPEP 2144.05).

Response to Arguments

13. Applicant's arguments filed 1/17/2005 have been fully considered but they are not persuasive.

Applicant's argument that all of the independent claims require both the bond area and the probe portion to be on the semiconductor chip itself and not on the wafer scribe lanes between chips, which is not taught by the prior art is noted but is not found persuasive. The claims merely require a second portion including a probe area on the semiconductor chip for providing contact with a probe for device testing, note claim 10. Kim et al teaches a plurality of wafer probing pads **38** formed on the **chip** scribe lanes **34**. Kim et al teaches forming on the chip scribe lanes, which based on the broadest reasonable interpretation meets the claimed limitation of "on the chip" because the scribe lanes are a part of the chip, as taught by Kim et al. The limitation of "on the semiconductor chip" does not overcome the prior art because the boundaries of the chip have not been defined to exclude the scribe lanes, which based on the broadest reasonable interpretation of "semiconductor chip" would include the scribe lanes because Kim et al teaches "chip scribe lanes". It is also noted that the final chip cut from the wafer also a portion of the bond pad, which meets the limitation required for the probe pad. The probe pad is required to be disposed over a dielectric layer and offset from the metal line. Kim et al teaches a bond pad **56** with a portion of the bond pad overlying a dielectric layer and not overlying the metal line **52a** (Figs 5-6 and 9), which meets the claimed limitation of applicant's probe pad. Referring to claim 1, the probe pad is not positively recited to be required on the semiconductor chip. Only the bond pad is required to be on the chip, which is taught by Kim et al.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the bond area

and probe portion not on the wafer scribe lanes) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Besser et al (US 6,239,494) teaches a diffusion barrier comprising Ti, Ta, W, an alloy thereof or a nitride (col 4, ln 5-25) and an inter-dielectric layer comprises an oxide or a nitride (col 4, ln 60-67).

Chevallier (US 6,140,665) teaches a bonding mask and a probe make are separate (col 5, ln 45-600.

Sugasawara (US 5,936,876) teaches forming openings in a passivation layer to expose a probe pad (col 7, ln 1-25) and the probe pad is not connected to the bond pad (claim 1).

Ishikawa et al (JP 03-1516510 teaches a probe region and a bond pad region and the two part pad prevents damage to a wire bonding part (Abstract).

Buynoski (US 4,761,386) teaches a passivation layer (col 3, ln 5-25), probes contacting the bonding pads and bonding wire to the pads (col 4, ln 1-15).

Bell (US 6,429,675) teaches a first area for a bond pad and second area for a probe formed simultaneously (col 4, ln 10-30).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 571-272-1137. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1722

MJS
May 13, 2005

ROBERT KUNEMUND
PRIMARY EXAMINER